1. A linear ramp generation circuit operating in a recovery mode, a ramp mode, or a hold mode, said circuit comprising:

an output node;

a first input node coupled to an externally provided first input signal;

a second input node coupled to an externally provided second input signal;

a constant current source network;

a capacitor having a first node and a second node, the first node being maintained at a circuit reference level, the second node being coupled to the output node at least during the hold mode of operation;

a return charge network for returning a voltage on the capacitor to a baseline level during the recovery mode;

a first switch means responsive to the first input signal for connecting the second node of the capacitor to the constant current source network during the ramp mode of operation and changing the voltage on the capacitor away from the baseline level, and for uncoupling the second node of the capacitor from the constant current source network during the hold mode and recovery mode of operation; and

a second switch means responsive to the second input signal for connecting the second node of the capacitor to said return charge network during the recovery mode of operation to return the voltage on the capacitor to the baseline level, and for uncoupling the second node of the capacitor from the return charge network during the ramp mode and hold mode of operation.

2. A linear ramp generation circuit of claim 1, wherein the return charge network recharges the capacitor during the recovery mode of operation.

3. A linear ramp generation circuit of claim 1, wherein the return charge network includes an active-feedback circuit which implements an approximately second-order voltage response to the capacitor during the recovery mode of operation.

4. A linear ramp generation circuit of claim 1, wherein the output node is coupled to the second node of the capacitor through a composite amplifier including a FET pair and an op-amp.

5. A linear ramp generation circuit of claim 1, wherein the first node of the capacitor is at a circuit ground reference voltage.

6. A linear ramp generation circuit of claim 1, wherein the constant current source network includes an op-amp.

7. A linear ramp generation circuit of claim 1, wherein the first and second switch means are differential-paired transistors.

8. A linear ramp generation circuit of claim 1, wherein the return charge network includes an op-amp and an associated impedance feedback network.

9. A linear ramp generation circuit operating in a discharge mode, a hold mode, or a recovery mode, said circuit comprising:

a first input node and a second input node for receiving a first input signal and a second input signal, respectively;

an output node;

a constant current source network;

a recharge network having a first node and a second node, the first node of the recharge network connected to the output node;

a capacitor having a first node and a second node, the first node of the capacitor being maintained at a circuit reference level, and the second node of the capacitor being coupled to the output node at least during the hold mode of operation;

a first transistor switch responsive to the first input signal for connecting the second node of the capacitor to the constant current source network during the discharge mode of operation and for uncoupling the second node of the capacitor from the constant current source network during the hold mode and recovery mode of operation; and

a second transistor switch responsive to the second input signal for connecting the second node of the capacitor to the second node of the recharge network during the recovery mode of operation and for uncoupling the second node of the capacitor from the second node of the recharge network during the discharge mode and hold mode of operation.

10. A linear ramp generation circuit of claim 9, wherein the recharge network includes an active-feedback circuit which implements an approximately second-order voltage response to the capacitor during the recovery mode of operation.

11. A linear ramp generation circuit of claim 9, wherein the constant current source network is a current sink for linearly discharging the capacitor during the discharge mode of operation.

12. A linear ramp generation circuit of claim 9, wherein the first node of the capacitor is at a circuit ground reference voltage.

13. A linear ramp generation circuit of claim 9, wherein the first transistor switch and second transistor switch are differential-paired transistors.

14. A linear ramp generation circuit of claim 9, wherein the recharge network includes an op-amp and an associated impedance feedback network.

15. A linear ramp generation circuit of claim 9, wherein the output node is coupled to the second node of the capacitor through a composite amplifier including a FET pair and an op-amp.

16. A linear ramp generation circuit for operating in a ramp mode, a hold mode, or a recovery mode, said circuit comprising:

a first input node and a second input node for receiving a first input signal and a second input signal, respectively;

an output node;

a current network providing a constant current;

a return charge network having a first node connected to the output node and a second node connected to a control node;

a capacitor having a first node and a second node, the first node being maintained at a circuit reference level, and the second node being coupled to the output node at least during the hold mode of operation;

a current steering element responsive to the first input signal for connecting the current network to the second node of the capacitor during the ramp mode of operation and for connecting the current network to a different node during the hold mode and recovery mode of operation; and

a transistor switch responsive to the second input signal for coupling the control node of the return charge network to the second node of the capacitor during the recovery

mode of operation and for uncoupling the control node from the capacitor during the ramp mode and hold mode of operation.

17. A linear ramp generation circuit of claim 16, wherein the return charge network includes an active-feedback circuit for recharging the capacitor during the recovery mode of operation.

18. A linear ramp generation circuit of claim 17, wherein the return charge network implements an approximately second-order voltage response to the capacitor during the recovery mode of operation.

19. A linear ramp generation circuit of claim 16, wherein the current steering element includes differential-paired transistors.

20. A method of sequentially operating a linear ramp generation circuit, said method comprising the steps of:

upon the occurrence of a first input signal, discharging a capacitor having a first node and a second node from an initial baseline voltage level by connecting a constant current source network to the second node of the capacitor, said first node being maintained at a circuit reference level;

upon the occurrence of a second input signal, disconnecting the second node of the capacitor from the constant current source network;

maintaining the second node of the capacitor at a high impedance during a hold period after the occurrence of the second input signal;

connecting the second node of the capacitor during the hold period to an output node;

upon the occurrence of a third input signal, connecting the second node of the capacitor to a recovery network for recharging the capacitor back to the baseline voltage level; and

upon the occurrence of a fourth input signal, disconnecting the first node of the capacitor from the recovery network prior to a succeeding first input signal.

21. The method of claim 20, further comprising the step of:

upon the occurrence of the third input signal, coupling the second node of the capacitor through a composite amplifier including a FET pair and an op-amp.